oreboot 2022 status report
on to RISC-V

Daniel Maslowski
Hey Again OSFC!
Remember oreboot?
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oreboot is a fork of coreboot…
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From aa246f71de7f9900a30d938ab618c46839436616 [...] From: "Ronald G. Minnich" <rminnich@gmail.com> Date: Mon, 1 Apr 2019 23:48:56 +0000 Subject: [PATCH] Initial removal of C code
oreboot is firmware in Rust!

oreboot is a fork of coreboot, with C removed, written in Rust.

https://github.com/oreboot
State of Development in 2022 / Q4

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  - Got rid of a lot of boilerplate
  - Build speed increased with shared cache
  - Can still be built from toplevel or board dir running `make`
  - Removed FSP bits and everything but Allwinner D1 (sunxi/nezha)
  - References kept in a `graveyard.md` for revival
- Main focus is on RISC-V now
  - Build setup based on `xtask`
  - Driver model discarded in favor of Rust `embedded-hal`
- Website and documentation are being worked on.
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   23 files changed, 2 insertions(+), 13005 deletions(-)
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```

Removals are documented in graveyard.md.
Firmware Matryoshka

- initialize
  - oreboot ROM
  - oreboot RAM
  - oreboot dtfs

- payload
  - Linux
  - u-root
    - This is our bootloader environment, a Linux userland as initramfs.
  - dtb for Linux

- XIP/SRAM
- DRAM
- what didn't fit in SRAM
- extract payload
- setup handlers
- runpayload (done)
Firmware Matryoshka

Stages

- XIP/SRAM
  - early initialization
  - PLLs, clocks, GPIOs
  - UART, say hello
  - SPI flash MMIO
  - DRAM controller

- DRAM
  - what didn’t fit in SRAM
  - extract payload
  - set up handlers
  - run payload (done)
Firmware Runtime Services
Benefits

...for attackers—oops! Closed source means we can hardly fix issues on our own, while OEMs are slow to push out updates.
### Benefits

#### Vulnerability REsearch

<table>
<thead>
<tr>
<th>Vulnerability Category</th>
<th>Count</th>
<th>Average Impact</th>
</tr>
</thead>
<tbody>
<tr>
<td>PEI Memory Corruption</td>
<td>3</td>
<td>CVSS: 8.0 (High)</td>
</tr>
<tr>
<td>SMM Memory Corruption</td>
<td>49</td>
<td>CVSS: 8.0 (High)</td>
</tr>
<tr>
<td>DXE Memory Corruption</td>
<td>7</td>
<td>CVSS: 7.7 (High)</td>
</tr>
<tr>
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RISC-V Runtime Services: SBI

RISC-V Runtime Services are listed in the platform specification, referencing the SBI specification. The SBI (Supervisor Binary Interface) specification is a living document: https://github.com/riscv-non-isa/riscv-sbi-doc. It defines extensions and functions similar to system calls. Arguments and extensions/functional calls are passed through A registers. Then the call is performed via the ECALL instruction. Example, writing a B character to the serial console:

```
li a0, 'B' # argument
li a7, 0x01 # extension "console putchar"
ecall
```

Ports need to be written per platform (core/SoC/board).
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RustSBI

RustSBI is a library for implementing a specific platform SBI solution based on Rust. This library adapts to embedded Rust's `embedded-hal` crate to provide basic SBI features. When building for an own platform, implement traits in this library and pass them to the functions beginning with `init`. When handlers are set up, call `enter_privileged` to enter the OS in S-Mode.

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Porting sunxi/nezha
Allwinner Nezha Board

https://linux-sunxi.org/Allwinner_Nezha
Allwinner D1

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We can boot Linux. /o/
And xv6, MnemOS, r9—witheven more to come.
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RustSBI in reboot: example

```rust
pub fn sbi_exec(payload_offset: usize, dtb_offset: usize) -> ! {
    let hartid = riscv::register::mhartid::read();
    init_pmp();
    init_csrs();
    runtime::init();
    if hartid == 0 {
        init_plic();
        peripheral::init_peripheral();
    }
    delegate_interrupt_exception();
    // NOTE: This sets up handlers for SBI calls and traps
    execute_supervisor(payload_offset, hartid, dtb_offset)
}
```
Credits

We are very grateful for Rust SBI. It makes our life a lot easier. :) Mr Yang Derui, Vivian Wang and Luo Jia helped us out to get going. Paul Ruizendaal translated the DRAM init from an assembly dump to C, which we in turn based our Rust implementation on. Mimoja wrote and ran a full DRAM test ranging over the entire address space. Samuel Holland took the effort to pick up Allwinner's BSP, work out changes for mainline, and upstream patches to U-Boot, OpenSBI and Linux, joined our Nezha online community meetup, and continuously helped us out when we had questions or ran into issues. Michael Engel ported xv6 to the D1, which made an nice and small test payload. The D1 Mainline Telegram group with all its members had always been supportive. Special shoutout to Pierce who kept believing in our success!
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let b = f.copy_into([(o >> 16) as u8, (o >> 8) as u8 % 256, o as u8 % 256]);
```
Things We Messed Up: Off-by-one at scale

```rust
def copy_into(x: [u8]) -> [u8]
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Rust analyzer says something about 256 being too much for u8.
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After another hour of looking again, we managed to figure it out and learned that Rust already drops the higher bits for foo as u8.
Things We Messed Up: Cache coherence

Unable to handle kernel paging request at virtual address fffffff92f74c2ba
Oops [#1]

Modules linked in:
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Well, that wasn't us, but it took a long time to find it.

https://github.com/rust-embedded/riscv/pull/107
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It seems to have been a copy-paste error. We ran into a very nasty bug in a reboot on the Allwinner D1 (C906) where an erratapatch in Linux relies on those two being zero.
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Awesome Demo
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