oreboot 2022 status report

on to RISC-V

Daniel Maslowski



Hey Again OSFC!



Remember oreboot?



Remember oreboot?

oreboot is a fork of coreboot...





OREBOOT



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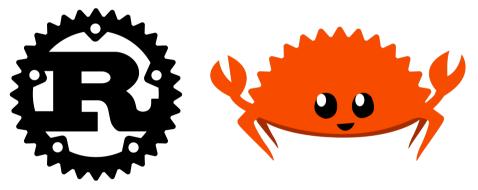
OREBOOT

From aa246f71de7f9900a30d938ab618c46839436616 [...]
From: "Ronald G. Minnich" <rminnich@gmail.com>
Date: Mon, 1 Apr 2019 23:48:56 +0000
Subject: [PATCH] Initial removal of C code



oreboot is firmware in Rust!

oreboot is a fork of coreboot, with C removed, written in Rust.



https://github.com/oreboot





🛈 reworked to Cargo Workspace, thanks to 洛佳 (Luo Ĵia)

- got rid of a lot of boilerplate
- build speed increased with shared cache
- can still be built from top level or board dir running make



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Website and documentation are being worked on.





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23 files changed, 2 insertions(+), 13005 deletions(-)



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Removals are documented in graveyard.md.

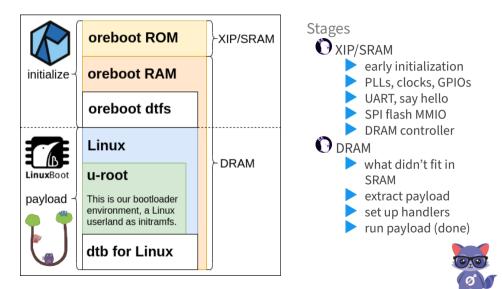


Firmware Matryoshka

	oreboot ROM	XIP/SRAM		
initialize -	oreboot RAM			
	oreboot dtfs			
	Linux	DDAM		
LinuxBoot	u-root	≻ DRAM		
payload -	This is our bootloader environment, a Linux userland as initramfs.			
	dtb for Linux			



Firmware Matryoshka



Firmware Runtime Services



Benefits



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Vulnerability REsearch				
Vulnerabillity Category	Count	Average Impact		
PEI Memory Corruption	3	CVSS: 8.0 (High)		
SMM Memory Corruption	49			
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#DXE #Firmware #f	- ujitsu #HP #Lenovo #PEI #	#SMI #SMM #UEFI			

... for attackers - whoops! Closed source means we can hardly fix issues on our own, while OEMs are slow to push out updates.





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Example, writing a **B** character to the serial console:

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eca	all					

Ports need to be written per platform (core/SoC/board).



OpenSBI



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An SBI written in C: https://github.com/riscv-software-src/opensbi



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R riscv-software-src / open	Sbi ⊙ Watch 51 + 🔮 Fork 253 🗲	Z Star 437 →
<> Code ① Issues 32 11	Pull requests 7 💿 Actions 🖽 Projects 🖽 W	/iki ···
🐉 master 👻 opensbi / platfo	orm / Go to file A	.dd file ▾ ····
Jan Remes and avpatel platfo	orm: generic: check if CPU node is enabled 12 days	ago 🕤 History
andes/ae350	lib: utils/serial: support 'reg-offset' property	last month
🖿 fpga	lib: utils/serial: support 'reg-offset' property	last month
🖿 generic	platform: generic: check if CPU node is enabled	12 days ago
kendryte/k210	include: sbi_utils: Introduce an helper to get fdt base ad	7 months ago
nuclei/ux600	include: sbi_utils: Introduce an helper to get fdt base ad	7 months ago
template	lib: utils/serial: support 'reg-offset' property	last month



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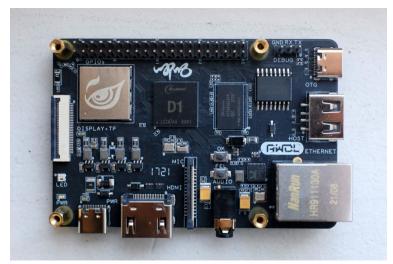
https://docs.rs/rustsbi/latest/rustsbi/



Porting sunxi/nezha



Allwinner Nezha Board



https://linux-sunxi.org/Allwinner_Nezha





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Status We can boot Linux. \o/ And xv6, MnemOS, r9 - with even more to come.



RustSBI in oreboot: example

```
pub fn sbi_exec(payload_offset: usize, dtb_offset: usize) -> ! {
    let hartid = riscv::register::mhartid::read();
    init pmp();
    init_csrs();
   runtime::init();
    if hartid == 0 {
        init_plic();
        peripheral::init peripheral();
    }
    delegate interrupt exception();
    // NOTE: This sets up handlers for SBI calls and traps
    execute supervisor(payload offset, hartid, dtb offset)
}
```





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The D1 Mainline Telegram group with all its members had always been supportive.

Special shoutout to Pierce who kept believing in our success!





let b = f.copy_into([(o >> 16) as u8, (o >> 8) as u8 % 256, o as u8 % 256]);



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After another hour of looking again, we managed to figure it out and learned that Rust already drops the higher bits for foo as u8.





Unable to handle kernel paging request at virtual address ffffff92f Oops [#1]

Modules linked in:

CPU: O PID: 103 Comm: kworker/0:0 Not tainted 5.19.0-rc1-14138-g4e54 Hardware name: Sipeed Lichee RV Dock (DT)

epc : wq_worker_running+0xa/0x56

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https://github.com/rust-embedded/riscv/pull/107 Fix reading marchid and mimpid It seems to have been a copy-paste error. We ran into a very nasty bug in oreboot on the Allwinner D1 (C906) where an errata patch in Linux relies on those two being zero.



Awesome Demo



Thank you!

