oreboot on RISC-V

Comparing Implementations on Two Platforms

Daniel Maslowski

Agenda

- Introduction
- Allwinner D1
- StarFive JH7100
- Approaches and Future Work

What is oreboot again?

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oreboot is a fork of coreboot…

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coreboot

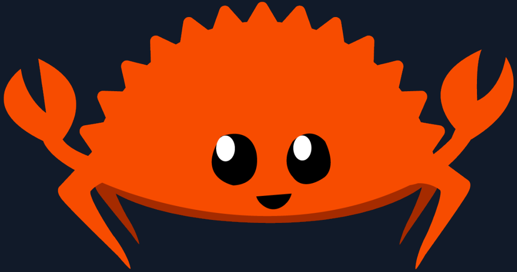
OREBOOT

```
From aa246f71de7f9900a30d938ab618c46839436616 [...]
From: "Ronald G. Minnich" <rminnich@gmail.com>
Date: Mon, 1 Apr 2019 23:48:56 +0000
Subject: [PATCH] Initial removal of C code
```

https://github.com/oreboot/oreboot

Firmware in Rust

oreboot is a fork of coreboot, with C removed, written in Rust.



Rust logo under CC BY 4.0, https://github.com/rust-lang/rust-artwork

Ferris the crab from https://rustacean.net/

Firmware Development

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feels like an RPG

You need to figure out how things work.

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Internet of Things = MMORPG

Yes, it can get very dangerous.

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- *open* tools for flashing, debugging and image composition
- firmware, *from the start*, documented (U-Boot, oreboot, …)
- Linux or other OS, *mainline friendly* (git fork, *not* source dump)
- all code usable with upstream toolchains, or provide toolchains in a *reproducible* form (not only binaries for a specific architecture/OS)

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OSHWA Certification: https://certification.oshwa.org/

Let’s look at a manual and a memory map!

Allwinner D1

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- widely produced and easily available
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Documentation

- larger manual provided
  - about 1400 pages
- DRAM controller and HDMI missing

D1 Boards and SoMs

Allwinner Nezha
first board; Raspberry Pi form factor

DongshanPi Nezha STU
- SoM in custom form factor
- carrier board with many pins

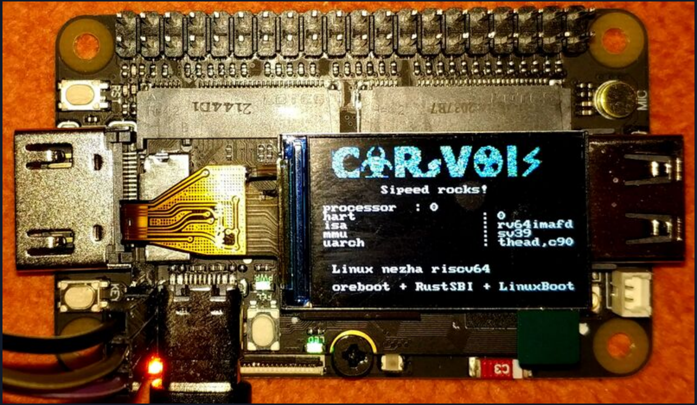
Sipeed Lichee RV
SoM and multiple carrier boards

ClockworkPi R01
- SoM in RPi CM 3 form factor
- DevTerm carrier board + case

MangoPi MQ-Pro
Raspberry Pi Zero form factor, drop-in replacement

https://linux-sunxi.org/Category:D1_Boards

D1 Boards: Lichee RV + Dock



```
processor   : 0
hart        : 0
isa         : rv64imafd
mmu         : sv39
uarch       : thead,c90

Linux nezha riscv64
oreboot + RustSBI + LinuxBoot
```

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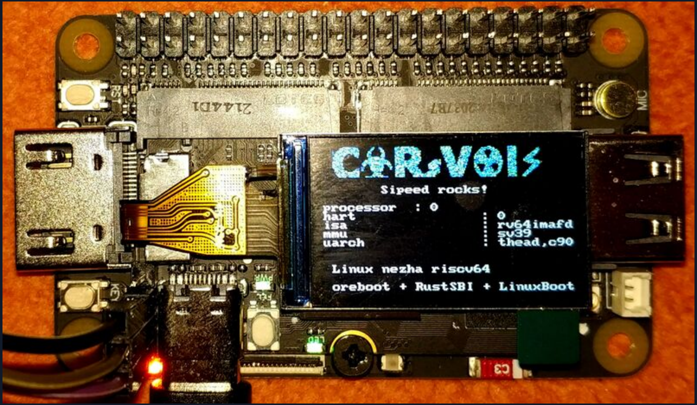

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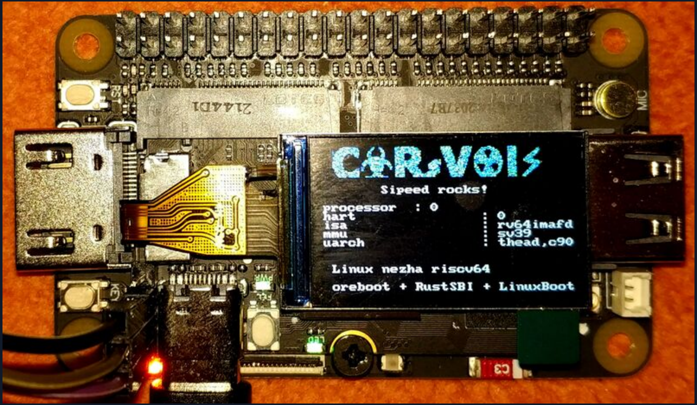

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The Dock Pro already has a 16 MiB SPI flash, plus a USB serial converter.

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Disassembly of section .head:

0000000000020000 <head_jump>:
   20000: a5 a0          j       0x20068 <start+0x8>
   20002: 00 00          unimp

0000000000020004 <_ZN17oreboot_nezha_bt09EGON_HEAD17h5aa4b41b712905f
   20004: 65 47 4f 4e 2e 42 54 30        eGON.BT0
   2000c: 39 6c 0a 5f 00 00 00 00        9l._....
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Note: The header is not documented in the manual.

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SPI flash

We need to actively read from SPI flash and have no MMIO access to it.

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SRAM Stage

Boot from flash and DRAM init were prototyped separately:
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Payloader Stage

First RustSBI implementation in oreboot is for Allwinner Nezha (D1):
`src/mainboard/sunxi/nezha/main`

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I tried my best to name registers; reviews and help wanted!

We may be able to reuse at least parts, and apply them to other Allwinner SoCs.

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- MnemOS
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more to come: FreeBSD, Illumos…

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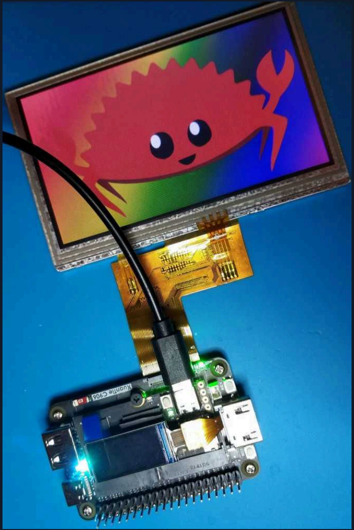
Bare metal testing app

https://github.com/adamgreig/d1rgb



StarFive JH7100

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Cores

- 2x U74 core, >1GHz
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Documentation

- no full manual publicly available
- instructions for firmware recovery with open tools
- sparse datasheet with list of peripheral blocks and suppliers (p23)
  - less than 140 pages

https://github.com/starfive-tech/JH7100_docs

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BeagleV

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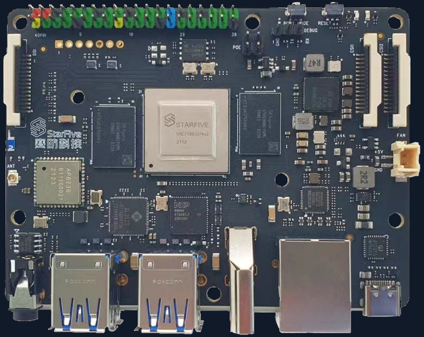
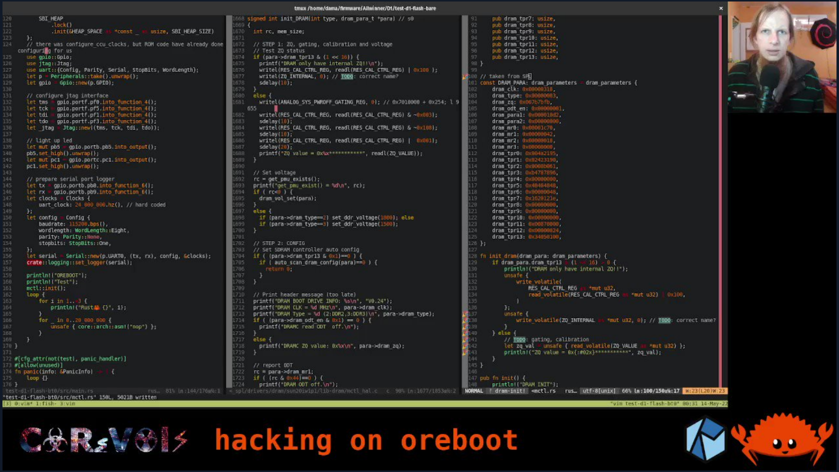
StarFive VisionFive 1



obtained via RISC-V International developer program
https://riscv.org/risc-v-developer-boards/details/

JH7100 Development Stream

Live: https://twitch.tv/cyrevolt



tmux /home/dama/firmware/Allwinner/D1/test-d1-flash-bare

```rust
        SBI_HEAP
            .lock()
            .init(&HEAP_SPACE as *const _ as usize, SBI_HEAP_SIZE)
    };
    // there was configure_ccu_clocks, but ROM code have already done
 configuring for us
    use gpio::Gpio;
    use jtag::Jtag;
    use uart::{Config, Parity, Serial, StopBits, WordLength};
    let p = Peripherals::take().unwrap();
    let gpio = Gpio::new(p.GPIO);

    // configure jtag interface
    let tms = gpio.portf.pf0.into_function_4();
    let tck = gpio.portf.pf5.into_function_4();
    let tdi = gpio.portf.pf1.into_function_4();
    let tdo = gpio.portf.pf3.into_function_4();
    let _jtag = Jtag::new((tms, tck, tdi, tdo));

    // light up led
    let mut pb5 = gpio.portb.pb5.into_output();
    pb5.set_high().unwrap();
    let mut pc1 = gpio.portc.pc1.into_output();
    pc1.set_high().unwrap();

    // prepare serial port logger
    let tx = gpio.portb.pb8.into_function_6();
    let rx = gpio.portb.pb9.into_function_6();
    let clocks = Clocks {
        uart_clock: 24_000_000.hz(), // hard coded
    };
    let config = Config {
        baudrate: 115200.bps(),
        wordlength: WordLength::Eight,
        parity: Parity::None,
        stopbits: StopBits::One,
    };
    let serial = Serial::new(p.UART0, (tx, rx), config, &clocks);
    crate::logging::set_logger(serial);

    println!("OREBOOT");
    println!("Test");
    mctl::init();
    loop {
        for i in 1..=3 {
            println!("Rust🦀 {}", i);
        }
        for _ in 0..20_000_000 {
            unsafe { core::arch::asm!("nop") };
        }
    }
}

#[cfg_attr(not(test), panic_handler)]
#[allow(unused)]
fn panic(info: &PanicInfo) -> ! {
    loop {}
}
```

```
test-d1-flash-bt0/src/main.rs        rus… 81% ln:144/176≡%:1
"test-d1-flash-bt0/src/mctl.rs" 150L, 5021B written
[3] 0:vim* 1:fish- 3:vim
```

```c
signed int init_DRAM(int type, dram_para_t *para) // s0
{
  int rc, mem_size;

  // STEP 1: ZQ, gating, calibration and voltage
  // Test ZQ status
  if (para->dram_tpr13 & (1 << 16)) {
    printf("DRAM only have internal ZQ!!\n");
    writel(RES_CAL_CTRL_REG, readl(RES_CAL_CTRL_REG) | 0x100 );
    writel(ZQ_INTERNAL, 0); // TODO: correct name?
    sdelay(10);
  }
  else {
    writel(ANALOG_SYS_PWROFF_GATING_REG, 0); // 0x7010000 + 0x254; l 9
655
    writel(RES_CAL_CTRL_REG, readl(RES_CAL_CTRL_REG) & ~0x003);
    sdelay(10);
    writel(RES_CAL_CTRL_REG, readl(RES_CAL_CTRL_REG) & ~0x100);
    sdelay(10);
    writel(RES_CAL_CTRL_REG, readl(RES_CAL_CTRL_REG) |  0x001);
    sdelay(20);
    printf("ZQ value = 0X%x***********", readl(ZQ_VALUE));
  }

  // Set voltage
  rc = get_pmu_exists();
  printf("get_pmu_exist() = %d\n", rc);
  if ( rc<0 ) {
    dram_vol_set(para);
  }
  else {
    if (para->dram_type==2) set_ddr_voltage(1800); else
    if (para->dram_type==3) set_ddr_voltage(1500);
  }

  // STEP 2: CONFIG
  // Set SDRAM controller auto config
  if ( (para->dram_tpr13 & 0x1)==0 ) {
    if ( auto_scan_dram_config(para)==0 ) {
      return 0;
    }
  }

  // Print header message (too late)
  printf("DRAM BOOT DRIVE INFO: %s\n", "V0.24");
  printf("DRAM CLK = %d MHz\n", para->dram_clk);
  printf("DRAM Type = %d (2:DDR2,3:DDR3)\n", para->dram_type);
  if ( (para->dram_odt_en & 0x1) == 0 ) {
    printf("DRAMC read ODT  off.\n");
  }
  else {
    printf("DRAMC ZQ value: 0x%x\n", para->dram_zq);
  }

  // report ODT
  rc = para->dram_mr1;
  if ( (rc & 0x44)==0 ) {
    printf("DRAM ODT off.\n");
```

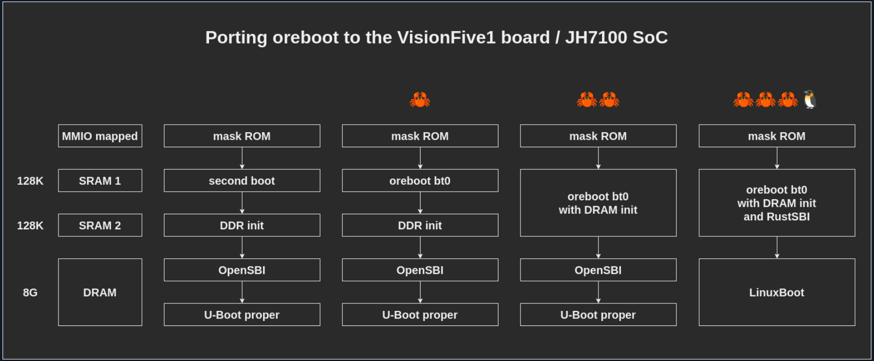
```
<_spl/drivers/dram/sun20iw1p1/lib-dram/mctl_hal.c   c  90% ln:1677/1853≡%:2
```

```rust
    pub dram_tpr7: usize,
    pub dram_tpr8: usize,
    pub dram_tpr9: usize,
    pub dram_tpr10: usize,
    pub dram_tpr11: usize,
    pub dram_tpr12: usize,
    pub dram_tpr13: usize,
}

// taken from SPL
const DRAM_PARA: dram_parameters = dram_parameters {
    dram_clk: 0x00000318,
    dram_type: 0x00000003,
    dram_zq: 0x007b7bfb,
    dram_odt_en: 0x00000001,
    dram_para1: 0x000010d2,
    dram_para2: 0x00000000,
    dram_mr0: 0x00001c70,
    dram_mr1: 0x00000042,
    dram_mr2: 0x00000018,
    dram_mr3: 0x00000000,
    dram_tpr0: 0x004a2195,
    dram_tpr1: 0x02423190,
    dram_tpr2: 0x0008b061,
    dram_tpr3: 0xb4787896,
    dram_tpr4: 0x00000000,
    dram_tpr5: 0x48484848,
    dram_tpr6: 0x00000048,
    dram_tpr7: 0x1620121e,
    dram_tpr8: 0x00000000,
    dram_tpr9: 0x00000000,
    dram_tpr10: 0x00000000,
    dram_tpr11: 0x00870000,
    dram_tpr12: 0x00000024,
    dram_tpr13: 0x34050100,
};

fn init_dram(dram_para: dram_parameters) {
    if dram_para.dram_tpr13 & (1 << 16) > 0 {
        println!("DRAM only have internal ZQ!!");
        unsafe {
            write_volatile(
                RES_CAL_CTRL_REG as *mut u32,
                read_volatile(RES_CAL_CTRL_REG as *mut u32) | 0x100,
            )
        };
        unsafe {
            write_volatile(ZQ_INTERNAL as *mut u32, 0); // TODO: correct name?
        }
    } else {
        // TODO: gating, calibration
        let zq_val = unsafe { read_volatile(ZQ_VALUE as *mut u32) };
        println!("ZQ value = 0x{:#02x}***********", zq_val);
    }
}

pub fn init() {
    println!("DRAM INIT");
```

```
NORMAL  ! dram-init!  <mctl.rs   rus…  utf-8[unix]  66% ln:100/150≡%:17  W:23(L20)W:23
                                             "vim test-d1-flash-bt0" 00:31 14-May-22
```

Archive: https://www.youtube.com/playlist?list=PLenOHeTI_A9PSGshDnEc4dYK-GSnCshk6

JH7100 Vendor Code and Transition Plan



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Note: Multiple cores allows for accessing peripherals in parallel.

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Note: Multiple cores allows for accessing peripherals in parallel.
Strategy: loop second hart; when done with peripherals, jump to OS.

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We reported the issue, with no reply so far.

https://github.com/starfive-tech/JH7100_ddrinit/issues/14

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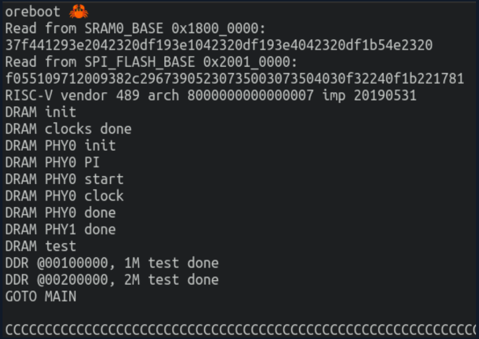

```
oreboot 🦀
Read from SRAM0_BASE 0x1800_0000:
37f441293e2042320df193e1042320df193e4042320df1b54e2320
Read from SPI_FLASH_BASE 0x2001_0000:
f055109712009382c2967390523073500307350403 0f32240f1b221781
RISC-V vendor 489 arch 8000000000000007 imp 20190531
DRAM init
DRAM clocks done
DRAM PHY0 init
DRAM PHY0 PI
DRAM PHY0 start
DRAM PHY0 clock
DRAM PHY0 done
DRAM PHY1 done
DRAM test
DDR @00100000, 1M test done
DDR @00200000, 2M test done
GOTO MAIN

CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
```

- pull request open with DRAM init and jump to next stage https://github.com/oreboot/oreboot/pull/606
- we currently load and jump to the U-Boot + OpenSBI blob
  - which can then load Linux, e.g., via network

Approaches and Future Work

Talking to peripherals

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Register Blocks

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```rust
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```

MMIO (memory-mapped input/output)

Writing to a peripheral register happens through a memory write instruction.
To change a value, read first, apply a mask, and write back.
Example:

```rust
unsafe {
  let peri0_ctrl = read_volatile(CCU_PLL_PERI0_CTRL as *mut u32);
  let new_val = peri0_ctrl | 1 << 29; // set bit `29`
  write_volatile(CCU_PLL_PERI0_CTRL as *mut u32, new_val);
}
```

SVD -> PAC -> HAL

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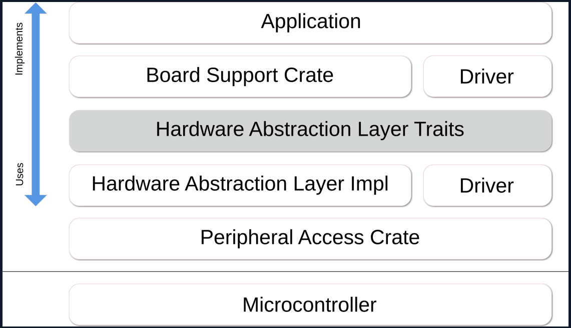

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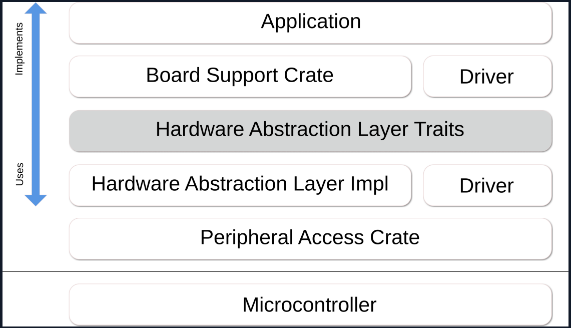

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Layers in oreboot

1. App (mainboard)
2. HAL (“drivers”)
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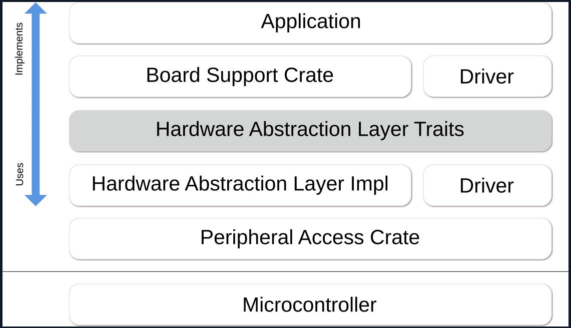

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Layers in oreboot

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2. HAL (“drivers”)
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PACs are commonly generated from SVD files.

https://docs.rust-embedded.org/book/portability/index.html

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// light up led
let mut pb5 = gpio.portb.pb5.into_output();
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```
ccu.smhc0_clk.write(|w| w.clk_src_sel().pll_peri_1x());
```

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In oreboot, we use RustSBI.
https://github.com/rustsbi/rustsbi
https://docs.rs/rustsbi/latest/rustsbi/

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Both CSRs and custom instructions may be neglected, and a subset of the SoC’s capabilities be used.

Potential RISC-V SoCs for oreboot

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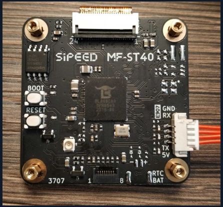
BL808

- already available (I have multiple boards)
- 1x C906 (512MHz), 1x E907, 1x low-power core



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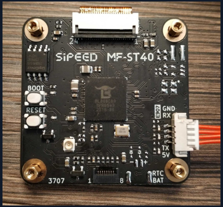

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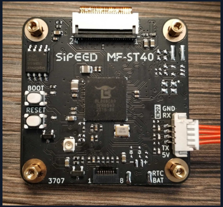

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TH1520

- SoM with SPI flash placeholder
- coming soon
- multiple boards offered https://sipeed.com/licheepi4a
  - Lichee Pi 4A
  - Lichee Cluster 4A
  - Lichee Router 4A
  - Lichee Pad/Phone 4A

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ARM and other ISAs

We had some ARM and x86 boards and discarded them in favor of getting on.
However, there are issues tracking their status with starting points.
https://github.com/oreboot/oreboot/issues

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Daniel Maslowski

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https://github.com/oreboot/oreboot

https://metaspora.org/oreboot-comparison-riscv-d1-jh7100.pdf